## REMARKS

This paper responds to the Office Action mailed on September 15, 2006.

Claims 1, 5, 8, 11, 18, 24, 49, 53, 57, 65-66, 68-69, 72-73, 76 and 78 are amended, claims 15-17, 21-23, 28-38, 43, 45, 47-48, 58-64 and 79 are canceled, and claims 80-95 are added; as a result, claims 1-14, 18-20, 24-27, 39-42, 44, 46, 49-57, 65-78, and 80-95 are now pending in this application.

Applicant has amended claims 1, 5, 8, 11, 18, 24 and 49 to more particularly point out and distinctly claim certain aspects of the present subject matter. Applicant respectfully submits that such amendments are fully supported by various portions of the specification, including the description at page 5, lines 2 and 16, page 6, lines 14-15 and 27, page 7, line 10, and figures 2-6.

Applicant has amended claim 24 to correct insufficient antecedent basis for the limitation "the multiple command and address pins." Applicant notes that such amendment was made to correctly identify dependence, and not in response to a prior art rejection of the claim.

Applicant has amended claims 53, 57, 72 and 76 to correct improper dependent form. Claim 53 was amended to correctly identify dependence on claim 51 instead of claim 52. Claim 57 was amended to correctly identify dependence on claim 55 instead of claim 56. Claim 72 was amended to correctly identify dependence on claim 70 instead of claim 71. Claim 76 was amended to correctly identify dependence on claim 74 instead of claim 75. Applicant notes that such amendments were made to correctly identify dependence, and not in response to a prior art rejection of the claims.

Applicant has amended claim 68 to correctly identify a component of the claim as "the controller," instead of "a controller." Applicant notes that such amendment was made to correctly identify a component, and not in response to a prior art rejection of the claim.

Applicant has amended claim 69 to correctly identify a component of the claim as "the first time," instead of "a first time." Applicant notes that such amendment was made to correctly identify a component, and not in response to a prior art rejection of the claim.

Applicant has amended claim 73 to correctly identify a component of the claim as "the second time," instead of "a second time." Applicant notes that such amendment was made to correctly identify a component, and not in response to a prior art rejection of the claim.

Applicant has amended claims 65-66 and 78 to correctly identify a component of the claim as "the programmable memory device," instead of "a programmable memory device." Applicant notes that such amendments were made to correctly identify a component, and not in response to a prior art rejection of the claims.

Accordingly, Applicant submits that no new matter has been introduced, and respectfully requests entry of the amendments to claims.

Applicant is presenting new claim 80. Applicant respectfully submits that such new claim 80 is fully supported by various portions of the specification, including the description at page 5, lines 2 and 16, page 6, lines 14-15 and 27, page 7, line 10, and figures 2-6.

Applicant is presenting new claims 81-82. Applicant respectfully submits that such new claims are fully supported by various portions of the specification, including the description and figures 2-6.

Applicant is presenting new claims 83-95. Applicant respectfully submits that such new claims are fully supported by various portions of the specification, including the description and figures 2-6, and the originally filed claims.

Applicant respectfully submits that such new claims 80-91 are fully supported by various portions of the specification, including the description and the figures, and the originally-filed claims. Therefore, Applicant submits that no new matter is introduced. Applicant respectfully requests consideration of and allowance of new claims 80-91.

Applicant further incorporates all prior responses by reference to preserve all issues for appeal and to focus the present response on the below comments that distinguish the presently claimed invention over the applied references.

*Claim Objections*

I. Claims 53, 57, 72 and 76 were objected to under 37 CFR 1.75(c), as being of improper dependent form for failing the infringement test. Applicant has amended these claims to overcome this objection. Applicant notes that such amendments were made to correct the improper dependent form, and not in response to a prior art rejection of the claims. Accordingly, Applicant respectfully requests entry of the amendments, and withdrawal of this objection to the claims.

II. Claim 78 was objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant respectfully traverses this objection. Claim 78, as amended, recites, "The method of claim 49, wherein the programmable memory device *consists of* J command and address pins." (*See* claim 78, emphasis added.) In contrast, claim 49 recites, in part, "receiving an F-bit word using J command and address pins of a programmable memory device." Applicant submits that claim 78 further limits the subject matter of claim 49. Accordingly, Applicant respectfully requests withdrawal of this objection to the claim.

*§112 Rejection of the Claims*

III. Claims 21-27, 45-46, 53, 57, 72 and 76 were rejected under 35 U.S.C. § 112, second paragraph, for indefiniteness. Applicant has canceled claims 21-23 and 45, thereby mooting this ground of rejection for said claims.

a. Claim 24 was rejected as having insufficient antecedent basis for the limitation "the multiple command and address pins." Applicant has amended claim 24 to correct the insufficient antecedent basis for the limitation. Accordingly, Applicant respectfully requests entry of the amendment to 24, and withdrawal of this rejection to claims 24-27 and 46. Applicant notes that such amendment was made to correct indefiniteness, and not in response to a prior art rejection of the claims.

b. Claims 53, 57, 72 and 76 were rejected as indefinite. Applicant has amended claims 53, 57, 72 and 76 to correct improper dependent form. Accordingly, Applicant respectfully requests entry of the amendments, and withdrawal of this rejection to the claims. Applicant notes that such amendments were made to correct indefiniteness, and not in response to a prior art rejection of the claims.

*§102 Rejection of the Claims*

IV. Claims 15-17, 21-23, 28-38, 43, 45 and 47-48 were rejected under 35 U.S.C. § 102(b) for anticipation by DeMone et al. (U.S. 6,266,750). Applicant has canceled claims 15-17, 21-23, 28-38, 43, 45 and 47-48, thereby mooting this ground of rejection for said claims.

*§103 Rejection of the Claims*

V. Claims 1-4, 39, 49-52, 54, 58-59, 61-71, 73 and 78-79 were rejected under 35 U.S.C. § 103(a) as being unpatentable over DeMone et al. (U.S. 6,266,750) and Schaefer (U.S. 5,666,321). Applicant has canceled claims 58-59, 61-64 and 79, thereby mooting this ground of rejection for said claims. With respect to the remaining claims, Applicant respectfully traverses.

a. Claim 1, as now amended, and in part, recites,

> receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, and wherein receiving the F-bit word comprises:

(*See* claim 1.) Applicant cannot find in DeMone et al. or Schaefer any disclosure, teaching, or suggestion of receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consist of an Active command, Bank Address signals, and Row Address signals, as recited in claim 1. Instead, address signals in DeMone et al. apparently include Row Addr data and Col Addr data (*see* fig. 2A), whereas in claim 1, address signals consist of only Bank Address signals and Row Address signals. Further, the cited portion of Schaefer apparently discloses address signals "compris[ing] a row address and a column-address," instead of address signals consisting of only Bank Address signals and Row Address signals. (*See* Schaefer at

column 1, line 31.) Thus, DeMone et al. and Schaefer fail to disclose, teach, or suggest receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consist of an Active command, Bank Address signals, and Row Address signals, as recited in claim 1.

Further, claim 1, in part, recites,

> receiving a second portion of the F-bit word substantially simultaneous with receiving a second edge of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of command and address signals;

(*See* claim 1.) Applicant cannot find in DeMone et al. or Schaefer any disclosure, teaching, or suggestion of receiving a second portion of the F-bit word substantially simultaneous with receiving a second edge of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of command and address signals, as recited in claim 1. The Office Action does not allege that DeMone et al. contains "where H is F-G". Further, the cited portion of Schaefer apparently discloses that "typical DRAM addresses are broken into two portions by an external logic control module (not depicted). These two portions comprise a row address and a column address . . . ." (*See* Schaefer at column 1, lines 29-32.) In contrast, claim 1 discloses "wherein the H-bit portion comprises a second subset of the set of command and address signals," wherein "the set of command and address signals consist of an Active command, Bank Address signals, and Row Address signals." (*See* claim 1.) Thus, where Schaefer requires a column address, claim 1 requires that there be only Bank Address signals and Row Address signals. Thus, DeMone et al. or Schaefer fails to disclose, teach, or suggest receiving a second portion of the F-bit word substantially simultaneous with receiving a second edge of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of command and address signals, as recited in claim 1.

Because all elements of claim 1 are not disclosed, taught, or suggested in DeMone et al. or Schaefer, Applicant respectfully submits that no *prima facie* case of obviousness presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 1.

With respect to dependent claims 2-4 and 39, Applicant respectfully submits that such claims include patentable subject matter beyond that recited in their respective base claims, and Applicant reserves the right to later present further remarks concerning such dependent claims.

b. Claim 49, as now amended, and in part, recites,

> receiving an F-bit word using J command and address pins of a programmable memory device, wherein F and J are positive integers, wherein J is less than F, wherein the F-bit word comprises a set of command and address signals, and wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals,

(*See* claim 49.) Applicant cannot find in DeMone et al. or Schaefer any disclosure, teaching, or suggestion of receiving an F-bit word using J command and address pins of a programmable memory device, wherein F and J are positive integers, wherein J is less than F, wherein the F-bit word comprises a set of command and address signals, and wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, as recited in claim 49. Instead, address signals in DeMone et al. apparently include Row Addr data and Col Addr data (*see* fig. 2A), whereas in claim 49, address signals consist of only Bank Address signals and Row Address signals. Further, the cited portion of Schaefer apparently discloses address signals "compris[ing] a row address and a column-address," instead of address signals consisting of only Bank Address signals and Row Address signals. (*See* Schaefer at column 1, line 31.) Thus, DeMone et al. and Schaefer fail to disclose, teach, or suggest receiving an F-bit word using J command and address pins of a programmable memory device, wherein F and J are positive integers, wherein J is less than F, wherein the F-bit word comprises a set of command and address signals, and wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, as recited in claim 49.

Further, claim 49, as now amended, and in part, recites,

> receiving a first portion of the F-bit word at a first time using G command and address pins, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein G is less than or equal to J, wherein the first portion of the F-bit word consists of a set of command signals and a first subset of address signals, wherein the set of command signals includes a Chip Select (CS#) signal, a Row Address Strobe (RAS#) signal, a Column Address Strobe (CAS#) signal, and a Write Enable (WE#) signal, wherein receiving the set of command signals includes using a set of Command Pins, wherein the set of Command Pins include a CS# pin, a RAS# pin, a CAS# pin, and a WE# pin, wherein receiving the first

subset of address signals includes using a set of Address Pins, and wherein the set of Address Pins include G-4 pins;

(*See* claim 49.) Applicant cannot find in DeMone et al. or Schaefer any disclosure, teaching, or suggestion of receiving a first portion of the F-bit word at a first time using G command and address pins, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein G is less than or equal to J, wherein the first portion of the F-bit word consists of a set of command signals and a first subset of address signals, wherein the set of command signals includes a Chip Select (CS#) signal, a Row Address Strobe (RAS#) signal, a Column Address Strobe (CAS#) signal, and a Write Enable (WE#) signal, wherein receiving the set of command signals includes using a set of Command Pins, wherein the set of Command Pins include a CS# pin, a RAS# pin, a CAS# pin, and a WE# pin, wherein receiving the first subset of address signals includes using a set of Address Pins, and wherein the set of Address Pins include G-4 pins, as recited in claim 49. Applicant cannot find in DeMone et al. any disclosure, teaching, or suggestion of receiving a Chip Select (CS#) signal, a Row Address Strobe (RAS#) signal, a Column Address Strobe (CAS#) signal, or a Write Enable (WE#) signal. Further, although Schaefer apparently discloses a RAS and a CAS, there is no reference to a Chip Select (CS#) signal or a Write Enable (WE#) signal. Moreover, Applicant cannot find in Demone et al. any disclosure, teaching, or suggestion of receiving a set of command signals and a first subset of address signals, where the set of address signals consists of Bank Address signals and Row Address signals. Thus, DeMone et al. or Schaefer fails to disclose, teach, or suggest receiving a first portion of the F-bit word at a first time using G command and address pins, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein G is less than or equal to J, wherein the first portion of the F-bit word consists of a set of command signals and a first subset of address signals, wherein the set of command signals includes a Chip Select (CS#) signal, a Row Address Strobe (RAS#) signal, a Column Address Strobe (CAS#) signal, and a Write Enable (WE#) signal, wherein receiving the set of command signals includes using a set of Command Pins, wherein the set of Command Pins include a CS# pin, a RAS# pin, a CAS# pin, and a WE# pin, wherein receiving the first subset of address signals includes using a set of Address Pins, and wherein the set of Address Pins include G-4 pins, as recited in claim 49.

Further yet, claim 49, as amended, and in part, recites,

> receiving a second portion of the F-bit word at a second time, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein H is less than or equal to J, and wherein the second portion of the F-bit word consists of a second subset of address signals;

(*See* claim 49.) Applicant cannot find in DeMone et al. or Schaefer any disclosure, teaching, or suggestion of receiving a second portion of the F-bit word at a second time, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein H is less than or equal to J, and wherein the second portion of the F-bit word consists of a second subset of address signals, as recited in claim 49. The Office Action does not allege that DeMone et al. contains "where H is F-G". Further, the cited portion of Schaefer apparently discloses that "typical DRAM addresses are broken into two portions by an external logic control module (not depicted). These two portions comprise a row address and a column address . . . ." (*See* Schaefer at column 1, lines 29-32.) In contrast, claim 49 discloses "wherein the second portion of the F-bit word consists of a second subset of address signals," wherein address signals consist of only Bank Address signals and Row Address signals. Thus, DeMone et al. or Schaefer fails to disclose, teach, or suggest receiving a second portion of the F-bit word at a second time, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein H is less than or equal to J, and wherein the second portion of the F-bit word consists of a second subset of address signals, as recited in claim 49.

Because all elements of claim 49 are not disclosed, taught, or suggested in DeMone et al. or Schaefer, Applicant respectfully submits that no *prima facie* case of obviousness presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 49.

With respect to dependent claims 50-52, 54, 65-71, 73 and 78, Applicant respectfully submits that such claims include patentable subject matter beyond that recited in their respective base claims, and Applicant reserves the right to later present further remarks concerning such dependent claims.

VI. Claims 5-14, 40-42, 55-56, 60, 74-75 and 77 were rejected under 35 U.S.C. § 103(a) as being unpatentable over DeMone et al., Schaefer and Ohshima et al. (U.S. Publication

2001/0006483). Applicant has canceled claim 60, thereby mooting this ground of rejection for claim 60. With respect to the remaining claims, Applicant respectfully traverses.

a. Claims 5, 8 and 11, as now amended, and in part, all recite,

> receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals,

(*See* claim 5.) Applicant cannot find in DeMone et al., Schaefer or Ohshima et al. any disclosure, teaching, or suggestion of receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, as recited in claims 5, 8 and 11. Instead, address signals in DeMone et al. apparently include Row Addr data and Col Addr data (*see* fig. 2A), whereas in claims 5, 8 and 11, address signals consist of only Bank Address signals and Row Address signals. Further, the cited portion of Schaefer apparently discloses address signals "compris[ing] a row address and a column-address," instead of address signals consisting of only Bank Address signals and Row Address signals. (*See* Schaefer at column 1, line 31.) In contrast, Ohshima et al. apparently teaches that the "distinction of row/column is not necessary any more, an address fetched by use of the first command is referred to as an upper address UA and an address fetched by use of the second command is referred to as a lower address LA in FIG. 8." (*See* Ohshima at ¶60.) Further, Applicant cannot find in DeMone et al., Schaefer or Ohshima et al. any disclosure, teaching, or suggestion of receiving an Active command as recited in claims 5, 8 and 11. Thus, DeMone et al., Schaefer or Ohshima et al. fail to disclose, teach, or suggest receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, as recited in claims 5, 8 and 11.

Because all elements of claims 5, 8 and 11 are not disclosed, taught, or suggested in DeMone et al. or Schaefer, Applicant respectfully submits that no *prima facie* case of

obviousness presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claims 5, 8 and 11.

With respect to dependent claims 6-7, 9-10, 12-13 and 40-42, Applicant respectfully submits that such claims include patentable subject matter beyond that recited in their respective base claims, and Applicant reserves the right to later present further remarks concerning such dependent claims.

b. With respect to dependent claims 55-56, 74-75 and 77, Applicant respectfully submits that such claims include patentable subject matter beyond that recited in their respective base claims, and Applicant reserves the right to later present further remarks concerning such dependent claims.

VII. Claims 18-20, 24-27, 44 and 46 were rejected under 35 U.S.C. § 103(a) as being unpatentable over DeMone et al. and Ohshima et al. Applicant respectfully traverses.

a. Claim 18, as amended, and in part, recites,

> multiple command and address pins to receive a first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals,

(*See* claim 18.) Applicant cannot find in DeMone et al. or Ohshima et al. any disclosure, teaching, or suggestion of multiple command and address pins to receive a first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, as recited in claim 18. Instead, address signals in DeMone et al. apparently include Row Addr data and Col Addr data (*see* fig. 2A), whereas in claim 18, address signals consist of only Bank Address signals and Row Address signals. Further, Ohshima et al. apparently teaches that the "distinction of row/column is not necessary any more, an address fetched by use of the first command is referred to as an upper address UA and an address fetched by use of the second command is referred to as a lower address LA in FIG. 8." (*See* Ohshima at ¶60.) Moreover, Applicant cannot find in DeMone et al. or Ohshima

et al. any disclosure, teaching, or suggestion of receiving an Active command as recited in claims 18. Thus, DeMone et al. or Ohshima et al. fail to disclose, teach, or suggest multiple command and address pins to receive a first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, as recited in claim 18.

Because all elements of claim 18 are not disclosed, taught, or suggested in DeMone et al. or Ohshima et al., Applicant respectfully submits that no *prima facie* case of obviousness presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 18.

With respect to dependent claims 19-20 and 44, Applicant respectfully submits that such claims include patentable subject matter beyond that recited in their respective base claims, and Applicant reserves the right to later present further remarks concerning such dependent claims.

b. Claim 24, as amended, and in part, recites,

> one or more integrated circuit memory devices operable for sending and receiving signals, wherein each of the integrated circuit memory devices operates to receive a first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals,

(*See* claim 24.) Applicant cannot find in DeMone et al. or Ohshima et al. any disclosure, teaching, or suggestion of one or more integrated circuit memory devices operable for sending and receiving signals, wherein each of the integrated circuit memory devices operates to receive a first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, as recited in claim 24. Instead, address signals in DeMone et al. apparently include Row Addr data and Col Addr data (*see* fig. 2A), whereas in claim 24, address signals consist of only Bank Address signals and Row Address signals. Further, Ohshima et al. apparently teaches that the "distinction of row/column is not necessary any more, an address fetched by use of the first command is referred to as an

upper address UA and an address fetched by use of the second command is referred to as a lower address LA in FIG. 8." (*See* Ohshima at ¶60.) Moreover, Applicant cannot find in DeMone et al. or Ohshima et al. any disclosure, teaching, or suggestion of receiving an Active command as recited in claims 24. Thus, DeMone et al. or Ohshima et al. fail to disclose, teach, or suggest multiple command and address pins to receive a first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, as recited in claim 24.

Because all elements of claim 24 are not disclosed, taught, or suggested in DeMone et al. or Ohshima et al., Applicant respectfully submits that no *prima facie* case of obviousness presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 24.

With respect to dependent claims 25-27 and 46, Applicant respectfully submits that such claims include patentable subject matter beyond that recited in their respective base claims, and Applicant reserves the right to later present further remarks concerning such dependent claims.

## CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 17 Nov '06

By _____
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**CERTIFICATE UNDER 37 CFR** 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 17 day of November 2006.

KATE GANNON
Name

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Signature